Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Previously presented): An imprinting apparatus comprising:

a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a (110) horizontal planar surface and vertical sidewalls of a wet chemical etched trench, the trench vertical sidewalls being aligned with (111) vertical lattice planes of the semiconductor substrate; and

a plurality of vertical structures disposed in the trench between the trench vertical sidewalls, a material of the vertical structures being different from a material of the semiconductor substrate,

wherein the plurality of vertical structures are spaced apart from each other and from the trench vertical sidewalls to form a mold that provides a pattern for imprinting.

Claim 2 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than a (110) horizontal lattice plane to form the trench.

Claim 3 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechcol and tetramethylammonium hydroxide.

Claim 4 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a material selected from one of a Group IV element, Group III-V elements, and Group II-VI elements, the semiconductor substrate being wet chemical etched along the (111) vertical lattice planes.

Claim 5 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench sidewalls have smooth surfaces relative to trench sidewalls that are dry chemical etched.

Claim 6 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench sidewalls have reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

Claim 7 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in the [110] direction.

Claim 8 (Currently amended): The imprinting apparatus of Claim 1, further comprising:

nano-scale thick layers of a first material alternating with a layer of the vertical structure material in the trench, the first material being different from the semiconductor substrate material and the vertical structure material, one of the first material layers being adjacent to the semiconductor substrate.

Claim 9 (Previously presented): The imprinting apparatus of Claim 8, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the vertical structure material being selected from silicon dioxide, silicon nitride and germanium.

Claims 10 – 11 (Cancelled).

Claim 12 (Original): The imprinting apparatus of Claim 1, wherein the mold pattern has a vertical structure spacing in one or both of a nanometer range and a micrometer range.

Claim 13 (Currently amended): A nano-imprinting apparatus comprising:

a semiconductor substrate having a horizontal (110) planar surface and ~~a plurality of~~ (111) vertical lattice planes intersecting the (110) planar surface;

sidewalls of a trench etched in the semiconductor substrate along spaced apart (111) vertical lattice planes ~~of the plurality~~ using wet chemical etching, such that the trench sidewalls are (111) vertical planes; and

a plurality of ~~nano-scale spaced~~ vertical structures disposed in the trench, the vertical structures being nano-scale spaced apart and spaced from the trench sidewalls, a vertical structure of the plurality having opposing sides and an end, a side of the vertical structure facing one of a side of an adjacent vertical structure and a trench sidewall, the end having a horizontal surface coplanar with the (110) planar surface of the semiconductor substrate, a material of the plurality of vertical structures being different from a material the semiconductor substrate,

wherein the plurality of vertical structures between the trench sidewalls provides a nano-scale pattern for nano-imprinting.

Claim 14 (Original): The nano-imprinting apparatus of Claim 13, wherein the trench is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than the (110) planar surface.

Claim 15 (Original): The nano-imprinting apparatus of Claim 14, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechcol and tetramethylammonium hydroxide.

Claim 16 (Original): The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a material selected from one of an element from Group IV, elements from Group III-V, and elements from Group II-VI.

Claim 17 (Currently amended): The nano-imprinting apparatus of Claim 13, wherein the ~~vertical~~ sidewalls of the trench have one or both of smooth sidewalls

and reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

Claim 18 (Original): The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in a [110] direction.

Claim 19 (Original): The nano-imprinting apparatus of Claim 13, wherein the vertical structures comprise a material selected from silicon, silicon dioxide, silicon nitride and germanium deposited in the trench by a chemical vapor deposition.

Claim 20 (Previously presented): The nano-imprinting apparatus of Claim 13, further comprising:

deposited nano-scale thick layers of a first material alternating with deposited nano-scale thick layers of the vertical structure material in the trench, the first material being different from the material of the semiconductor substrate and the vertical structure material, one of the first material layers being adjacent to the semiconductor substrate.

Claim 21 (Previously presented): The nano-imprinting apparatus of Claim 20, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the vertical structure material being selected from silicon dioxide, silicon nitride and germanium.

Claims 22 – 23 (Cancelled).

Claim 24 (Original): The nano-imprinting apparatus of Claim 13, wherein the nano-scale pattern has one or both of a vertical structure spacing that ranges from about 5 nm to about 100 μm and a vertical structure pitch that ranges from about 10 nm to about 200 μm.

Claims 25 - 42 (Cancelled).

Claim 43 (Previously presented): The imprinting apparatus of Claim 8, wherein the first material layers have a thickness that defines spaces between the vertical structures of the plurality and further defines spaces between each trench sidewall and a vertical structure of the plurality that is adjacent to the trench sidewall.

Claim 44 (Previously presented): The imprinting apparatus of Claim 8, wherein the vertical structure material layer has vertically extending portions that are the vertical structures of the plurality.

Claim 45 (Previously presented): The imprinting apparatus of Claim 8, wherein the first material layers and the vertical structure material layer define an internal depth of the imprinting apparatus.

Claim 46 (Previously presented): The imprinting apparatus of Claim 13, further comprising:

layers of a first material alternating with layers of the vertical structure material in the trench, the first material layers and the vertical structure material layers in the trench defining an internal depth of the imprinting apparatus.

Claim 47 (Previously presented): The imprinting apparatus of Claim 46, wherein the layers of vertical structure material have vertically extending portions that are the plurality of vertical structures.

Claim 48 (Previously presented): The imprinting apparatus of Claim 46, wherein the first material layers have a thickness that defines spaces between the vertical structures of the plurality and defines spaces between each trench sidewall and a vertical structure of the plurality adjacent to the trench sidewall.

Claim 49 (Previously presented): The imprinting apparatus of Claim 20, wherein the nano-scale thickness of the first material layers define spaces between the vertical structures of the plurality and define spaces between each trench sidewall and a vertical structure of the plurality adjacent to the trench sidewall.

Claim 50 (Currently amended): An imprinting apparatus comprising:

a ~~semiconductor~~ substrate that is a semiconductor polished in a [110] direction, the ~~semiconductor~~ substrate having a trench with ~~vertical~~ sidewalls that are vertical, the sidewalls being aligned with (111) vertical lattice planes of the ~~semiconductor~~ substrate; and

a plurality of vertical structures disposed in the trench between the sidewalls, a material of the vertical structures being distinct from a material of the ~~semiconductor~~ substrate,

wherein the vertical structures are spaced apart from each other and from the sidewalls of the trench to form a mold that provides a pattern for imprinting.

Claim 51 (Previously presented): The imprinting apparatus of Claim 50, further comprising:

a first material disposed in the trench that is different from the vertical structure material and the substrate material, the first material being between some of the vertical structures of the plurality to define spaces between the vertical structures, the first material further being between each sidewall of the trench and an adjacent vertical structure of the plurality to define spaces between the sidewalls and the adjacent vertical structures, the first material defining an internal depth of the imprinting apparatus.

Claim 52 (Previously presented): The imprinting apparatus of Claim 50, further comprising:

alternating layers of a first material and the vertical structure material in the trench, the first material being different from the vertical structure material and the substrate material, one of the first material layers being adjacent to the substrate, the alternating layers defining an internal depth of the imprinting apparatus.

Claim 53 (Previously presented): The imprinting apparatus of Claim 52, wherein the layers of the vertical structure material have vertical portions corresponding to the vertical structures of the plurality, a thickness of the first material layers defining spaces between the vertical structures of the plurality and

further defining spaces between each sidewall and a vertical structure of the plurality that is adjacent to the sidewall.

Claim 54 (Currently amended): An imprinting apparatus comprising:

a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a trench with ~~vertical~~ sidewalls that are vertical, the sidewalls being aligned with (111) vertical lattice planes of the semiconductor substrate;

a plurality of vertical structures disposed in the trench between the sidewalls, and

alternating layers of a first material and a second material in the trench, the second material layers having portions that extend vertically, the vertically extending portions being the plurality of vertical structures,

wherein the vertical structures are spaced apart from each other and from the sidewalls of the trench to form a mold that provides a pattern for imprinting.

Claim 55 (Currently amended): The imprinting apparatus of Claim 54, wherein one layer of the first ~~materials~~ material is adjacent to the semiconductor substrate in the trench, a thickness of the first material layers defines spaces between vertical structures of the plurality and further defines spaces between the sidewall of the trench and a vertical structure of the plurality that is adjacent to the sidewall.

Claim 56 (Previously presented): The imprinting apparatus of Claim 54, wherein each of the first material, the second material and a material of the semiconductor substrate are different from one another.

Claim 57 (Previously presented): The imprinting apparatus of Claim 54, wherein the alternating layers define an internal depth of the imprinting apparatus.